REMARKS

Claims 1 to 17 and 19 to 22 are pending in the present application. Claims 1, 11, 17, 19 and 20 have been amended in an effort to clarify the present invention.

Reconsideration of the Examiner's decisions and reexamination of this application are respectfully requested.

It is noted that in the Final Office Action mailed July 9, 2008, all of the claims were rejected under 35 USC §112, first paragraph. The claims have been amended with the intent to clarify the claims so as to comply with 35 USC §112, first paragraph. Claims 1, 10, 11 and 22 will be addressed specifically.

In the claims below, the double underlined words in bold indicate where support for the limitations can be found. References to the specification are to paragraph numbers in the published patent application. The foregoing references to the Figures and the specification are for illustration purposes only and not limitation.

Replicated below is currently amended claim 1.

1. (Currently amended) An apparatus **Figure 17** comprising:

a buffer **1660** for storing indications of events generated by a ~~plurality of ports of a~~ peripheral device **80**, events include at least one of any of the following: an interrupt; an internal flag; a status indication of completion of the read operation; an indication that a new header is waiting; an indication that a packet header is ready; an indication triggered at an end of header processing, a descriptor, or a set of descriptors; a completion indication as a received packet which includes an acknowledgment; an indication of reception of a frame for transmission; an indication that a EventMask bit is cleared, an indication that the EventMask bit is cleared; an indication that a predetermined minimum number of event completed, said apparatus for transferring indications of events **[0153]** ~~interrupts~~from the peripheral device to a host computer system, and

a controller having a preset condition for an application, said preset condition comprising one of: a determination that the buffer is full; a determination that at least a

predetermined plurality of indications is stored in the buffer; a predetermined period has elapsed; and a determination that at least one indication is stored in the buffer and that a predetermined period has elapsed, said controller for, in response to a preset condition being met based on said indications, generating a control data block from the information stored in the buffer and **[0153]** comprising a payload portion having a plurality of fields each corresponding to LCP channel **[0155]** ~~a port from said plurality of ports~~ and a header portion having an identifier for identifying the control data block, ~~moving the contents of the buffer to the payload portion of the control data block,~~ and sending the control data block to the host computer system via an LCP channel **[0155]** ~~one port of the plurality of ports~~.

The following additional comments can be made. The apparatus of claim 1 is clearly directed to the preferred embodiment in Figure 17. The peripheral device is adapter 80 which includes ISOC 120, both of which are part of the hosting system 10 and includes memory 60. That the buffer is "for storing indications of events" and "transferring indications of events" is clear from [0153] where it is stated that "Completion event indications are queued in the interrupt FIFO 1660". "LCP channel" has been substituted for "ports" since there is clear support for this in [0155]: "The ICB 1680 is a data structure transferred by the ISOC 120 to the memory 60 of the host 10 via a dedicated LCP channel." and "The payload portion comprises a plurality of fields each containing the identity of the LCP channel…".

Replicated below is claim 10 with the indications of where each element is located.

10. (previously presented) An apparatus **Figures 1, 2, 17** as claimed in claim 1, further comprising: a host processing system **10** having a memory **60**, a data communications interface **260** for communicating data between the host computer system and a data communications network, forming a data processing system for controlling flow of interrupts from the data communication interface to the memory of the host processing system.

It should be commented that the data communications interface is the interposer 260 which forms a part of the peripheral device 80.

Replicated below is claim 11.

11. (Currently amended) A method comprising transferring interrupts generated by ~~from~~ a peripheral device to a host computer system, the peripheral device having a plurality of ports, the steps of transferring interrupts comprising:

storing interrupts generated by said ~~ports of the~~ peripheral device in a buffer;

determining if a preset condition is met, said preset condition comprising any of: a determination that the buffer is full; a determination that at least a predetermined plurality of indications is stored in the buffer; a predetermined period has elapsed; and a determination that at least one indication is stored in the buffer and that a predetermined period has elapsed, said controller for, in response to a preset condition being met based on said indications;

in response to the preset condition being met, generating a control data block from the information stored in the buffer and comprising a payload portion having a plurality of fields each corresponding to a different LCP channel ~~port from said plurality of ports~~ and a header portion having an identifier for identifying the control data block;

~~moving the contents of the buffer to the corresponding fields of the payload portion;~~ and

sending the control data block to the host computer system via an LCP channel ~~one of the ports~~.

The comments with respect to claim 1 apply equally as well here. It is noted that the phrase "moving the contents of the buffer to the corresponding fields of the payload portion" has

been removed and replaced with other language indicating that the control data block is generated from the information stored in the buffer.

Lastly, claim 22 is replicated here and the comments made with respect to claim 10 apply equally well here.

> 22. (previously presented) An apparatus **Figures 1, 2, 17** as claimed in claim 21, further comprising: a host processing system **10** having a memory **60**, a data communications interface **260** for communicating data between the host computer system and a data communications network, forming a data processing system for controlling flow of interrupts from the data communication interface to the memory of the host processing system.

The prior art rejections have not been addressed due to the substantial rewriting of claims 17, 19, and 20.

Summary:

In view of all of the preceding remarks, it is submitted that all of claims 1 to 17 and 19 to 22 are in condition for allowance. Further action with respect to the present application is earnestly solicited.

Respectfully submitted,

Giora Biran et al.

By: /Ira D Blecker/
Ira D. Blecker
Registration No. 29,894
Law Offices of Ira D. Blecker, P.C.
206 Kingwood Park
Poughkeepsie, New York 12601
845-849-3686
Facsimile: 845-849-3688